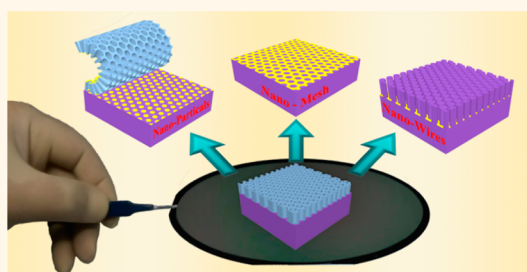


Facile Transferring of Wafer-Scale Ultrathin Alumina Membranes onto Substrates for Nanostructure Patterning

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ABSTRACT Ordered nanostructure arrays have attracted intensive attention because of their various applications. However, it is still a great challenge to achieve ordered nanostructure patterning over a large area (such as wafer-scale) by a technique that allows high throughput, large pattern area and low equipment costs. Here, through a unique design of the fabrication and transferring processes, we achieve a facile transferring of wafer-scale ultrathin alumina membranes (UTAMs) onto substrates without any twisting, folding, cracking and contamination. The most important in our method is fixing the UTAM onto the wafer-scale substrate before removing the backside Al and alumina barrier layer. It is also demonstrated that the thickness and surface smoothing of UTAMs play crucial roles in this transferring process. By using these perfectly transferred UTAMs as masks, various nanostructure patterning including nanoparticle, nanopore (nanomesh) and nanowire arrays are fabricated on wafer-scale substrates with tunable and uniform dimension. Because there are no requirements for UTAMs, substrates and materials to be deposited, the method presented here shall provide a cost-effective platform for the fabrication of ordered nanostructures on large substrates for various applications in nanotechnology.



KEYWORDS: wafer scale · nanostructure arrays · ultrathin alumina membranes

Ordered nanostructure arrays (patterns) have attracted intensive attention because of their important applications in various fields, such as in optoelectronics, energy conversion, sensing and storage.^{1–5} In order to achieve ordered nanostructure patterning over a large area for device applications, lithographical processes,^{6,7} imprinting techniques^{8–11} or self-assembly methods^{12–14} are adopted.^{15,16} Among them, expensive and complex equipment and costly imprinting stamps are requisite for lithographical processes and imprinting techniques. The self-assembly method is capable for cost-effective and large-scale nanostructuring, but usually suffers from low structural regularity and uniformity.¹³ Apart from these methods, template-based nanostructuring especially using anodized Al oxide (AAO) nanoporous template provides a cost-effective approach

for producing large scale nanostructure arrays or patterns with high regularity. Generally, AAO template is adopted for synthesizing one-dimensional nanostructure arrays in self-organized nanopore arrays^{1,2,15,17–19} or for replicating into metallic or semiconductor nanostructures.^{20–23} As a special AAO template, ultrathin alumina membrane (UTAM) can be used as a deposition or etching mask for achieving ordered nanoparticle arrays or surface patterns with nanopores on substrates.^{24–27} UTAM maintains the advantages of AAO template, including the uniformity and high density of self-organized nanopores, and the tunability of pore parameters (diameter, length and interspacing).²⁸ There are two types of UTAMs, namely connected and attached UTAMs.^{24,27} Although the connected UTAM has good adhesion with substrate and the capability to obtain nanopore arrays over

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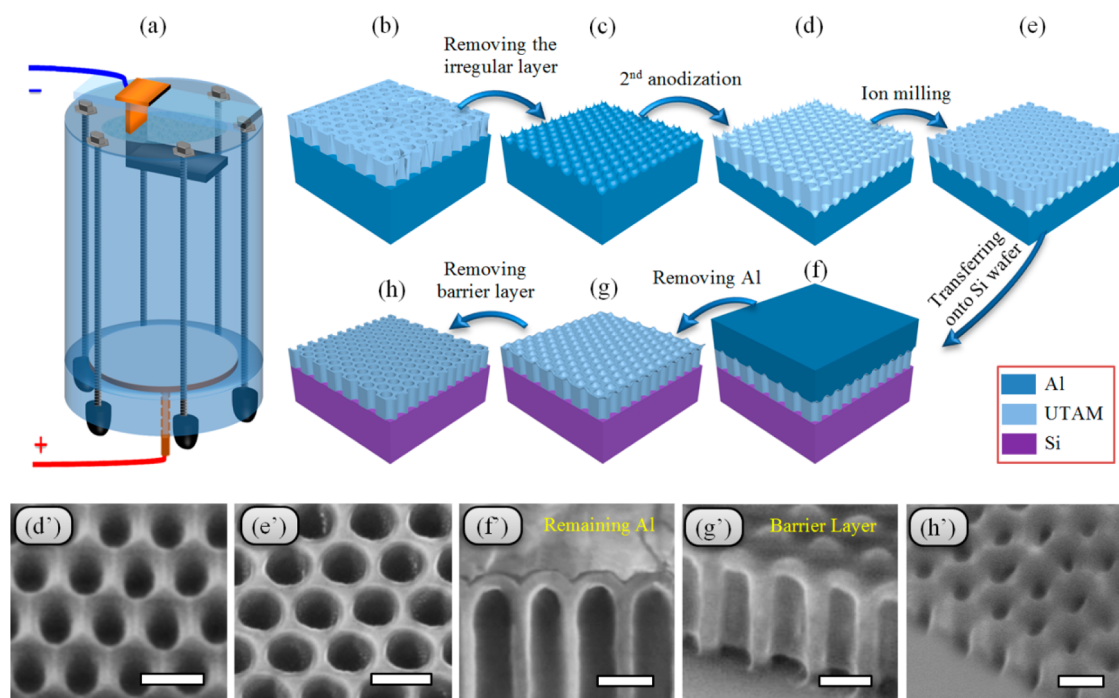


Figure 1. (a) Schematic diagram of the anodization and transferring cell for fabricating and transferring 4-in. sized UTAMs. (b–h) Schematic diagram and (d'–h') SEM images of the fabrication and transferring process of UTAM: (b) Al foil with irregular nanopores resulted from first anodization, (c) removing the irregular nanopores generated in first anodization, (d and d') regular nanopore arrays with sharp edges at the surface of the UTAM after second anodization, (e and e') regular nanopore arrays after ion-milling to smooth the surface of UTAM, (f and f') transferring the UTAM onto a Si wafer, (g and g') removing the residual Al at the backside, and (h and h') removing the barrier layer, leading to the UTAM on the Si wafer. (Scale bars in d'–h' are 100 nm).

large scale, its drawbacks of low regularity of nanopores and is difficult to remove the barrier layer completely,^{9–11} which limits its application potential. But the attached UTAM can be used to realize highly regular surface nanopatterns without the aforementioned problems for the connected UTAM, which makes the attached type more attractive for different applications.

Large-scale masking or patterning of an attached UTAM on a substrate is a great challenge.²⁶ Because of its ultrathin and fragile nature, direct transferring of free-standing UTAMs on substrates usually results in the twisting, folding or cracking of UTAMs, and hence an organic supporting layer (e.g., PMMA) is normally exploited for transferring the UTAM onto a substrate.^{8,26} However, this organic-assistant process could bring contaminations to the substrate and non-uniformity of UTAM pores. Moreover, after removing the organic layer, it is difficult to obtain a perfect and flat UTAM attached on a substrate with large area. Recently, we proposed a self-cleaning process to transfer UTAMs onto substrates without using an organic supporting layer,^{8,19} by which UTAMs with uniform pores were achieved without contaminations. However, free-standing membranes with area of only several mm² can be achieved by using this method, due to the ultrathin and fragile nature of UTAMs. Therefore, an efficient transferring process for large-scale

(cm² or even wafer scale) UTAMs on substrates is very important for the potential applications.

To address this issue, we report here a facile method, where highly ordered UTAMs over wafer-scale (4-in.) can be transferred onto substrates without any twisting, folding, cracking of UTAMs, as well as no contamination to the substrate. The treatment of the UTAM surface and reasonably fixing the UTAM onto the substrate before the removal of backside Al foil are essential to transfer large scale UTAMs successively. By using the transferred UTAMs as templates, various nanostructuring patterns were achieved over wafer scale, including nanoparticle, nanopore (nanomesh) and nanowire arrays with tunable and uniform dimension. Technically, there is no limit for the size of UTAM and no required prerequisites for UTAMs, substrates and the materials of the UTAM-prepared nanostructures (metals, insulators and semiconductors can be patterned), which will extremely extend the application of highly ordered nanostructure arrays. It should be noted that our method also can be used to prepare nanostructures with other symmetries in addition to hexagonal arrays, after prepatterning the Al surface prior to the anodization process.^{2,8,19,29}

RESULTS AND DISCUSSION

Highly ordered UTAMs are obtained by using a two-step anodization for polished Al foils according to the



Figure 2. Photographs of a 4-in. wafer-scale Al foil after surface polishing for UTAM preparation (a), as-prepared UATM on the Al foil (b), and the UATM transferred on a Si wafer (c).

literature.²⁶ Figure 1a shows the schematic diagram of the anodization and template-transferring cell for realizing 4-in. sized UTAMs. A long time anodization is necessary to form a regular hexagonal packed nanopore arrays with uniform shapes,³⁰ which is the reason that a two-step anodization is adopted for achieving highly ordered UTAMs. This also explains that irregular nanopore arrays are obtained in the aforementioned connected UTAMs because it is not physically feasible to deposit a rather thick Al film (at least dozens of micron) for a long anodization. After removal of the alumina obtained from the first anodization, a highly ordered nanohollow arrays are formed on the surface of the Al foil (Figure 1b,c). These highly ordered nanohollow arrays serve as a nucleation site for the development of a pore in the early stage of the second anodization,^{17,26} which results in the eventual growth of the UTAM with highly ordered pore channels (Figure 1d). In order to form a good attachment between the UTAM and substrate for following steps, the top surface of the UTAM is polished by ion milling before transferring. Figure 1d' shows a scanning electron microscopy (SEM) image of the top surface before polishing, which exhibits clear sharp edges at the triangle joint points of pore walls. After polishing, a smooth top surface of the UTAM is obtained, as shown in Figure 1e and 1e'. Because of increasing adhesion between the UTAM surface and substrate, this process of surface smoothing is indispensable for transferring UTAMs with large area on substrates without twisting and folding.

Because of the ultrathin and fragile nature of UTAMs, it is rather difficult to transfer an intact UTAM over large area on substrate. In our process, the UTAM is placed onto the desired substrate before removing the backside Al and the barrier layer (Figure S1 in Supporting Information). To avoid the moving of the UTAM during the following cleaning, pore opening and widening processes, the template is fixed on the substrate by using our anodization and transferring cell, which is crucial for keeping the membrane from twisting, folding and cracking. Several drops of DI water were

dropped on the substrate before attaching the UTAM, in order to further improve the contact of the membrane and the substrate. After these processes, the removals of backside Al and barrier layer were conducted successively (as shown in Figures S1, 1f, 1g and 1h), which resulted in a UTAM with highly ordered nanopore arrays attached on the substrate. Typical SEM images of UTAMs with backside Al, barrier layer and after removing the barrier layer are shown in Figures 1f', 1g' and 1h', respectively.

Figure 2 shows the successful transferring of a wafer-scale UTAM onto a Si substrate. It is clear that there is no any twisting, folding and cracking for the transferred UTAM. Because the membrane is fixed on the substrate during the whole process, the possible twisting or folding which may happen in the use of flexible polymeric supporting layer can be excluded. These twisting or folding will affect not only the final packing of the nanopores but also the uniformity due to the nonhomogenous contact with the pore-widening solution.⁸ The pore diameter of the obtained UTAM is about 70 nm, as shown in Figure 3a. The excellent contact of the UTAM and substrate, and the fixed UTAM during the following cleaning, pore-opening and -widening processes are two critical factors for transferring highly ordered UTAMs on the substrate with large area. It should be noted that there is no special requirement for the sizes (the cell and the substrate) in this process. Therefore, larger UTAMs also can be transferred successfully.

The successful transferring of UTAMs is dependent on their thickness and the diameter of the nanopores because thinner membrane with larger diameter of the nanopores means more fragile. If the thickness of the membrane is too thin, it will be broken even utilizing this method. Thick UTAM is beneficial for transferring but cannot pattern substrates successfully.²⁸ For further finding a suitable thickness that can guarantee an intact UTAM with a wafer scale during transferring onto the substrate, the dependences of the UTAM thickness on the anodization time and the diameter of nanopores in UTAMs on the pore-widening duration

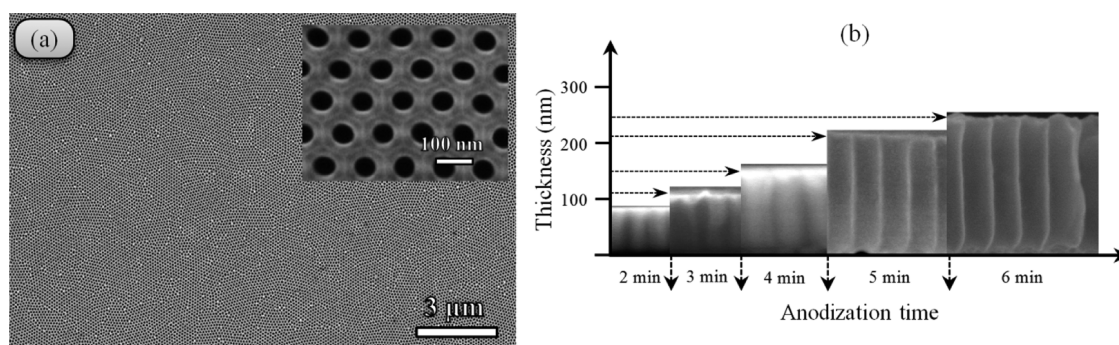


Figure 3. (a) Regional and high-resolution (inset) SEM images of the wafer-scale UTAM on Si substrate (top-view). (b) The dependence of the UTAM thickness on the second anodization time.

TABLE 1. Relationship of the Maximum Intact Area with the Thickness of UTAMs (Left Side) and the Dependence of the Nanopore Diameter in UTAMs on the Pore Widening Duration (Right Side)

relationship between the maximum intact area and the thickness of UTAM			relationship between the pore diameter and the pore widening duration	
second anodization time (min.)	thickness of UTAM (nm)	area of UTAM (cm ²)	pore widening duration (min.)	pore diameter (nm)
1	40–50	1	5	40
1.5	70–80	7	10	45
2	80–100	12	15	52.5
3	110–120	28	20	62
4	150–160	35	25	67
5	190–200	51	30	75
6	230–240	60	35	83.5
7	270–280	72	40	90
8	310–320	78 (~4 in.)	45	93.5

were systematically studied. Figure 3b shows the dependence of the UTAM thickness on anodization time. Table 1 shows two kinds of relationships, the relationship between the maximum intact areas and the thicknesses of UTAMs by controlling the anodization times, and the relationship between the pore diameters and the pore widening durations, which clearly exhibits the tunability of the pore diameter (also see Figure S2 in Supporting Information). It is clear that, in our condition, 8 min anodization (about 320 nm thickness of UTAM) is necessary for achieving an intact UTAM over 4-in. wafer scale. Furthermore, an intact free-standing 4-in. wafer scale UTAM with thickness about 500 nm can be fabricated, as shown in Figure S3 in Supporting Information.

To demonstrate the important applications of our novel method, nanoparticle arrays on a Si wafer were fabricated by using this UTAM as mask. Figure 4a outlines the fabrication of highly ordered nanoparticle arrays on large area substrate, including the transferred UTAM onto Si wafer, Au deposition and UTAM removing. After these steps, highly ordered Au nanoparticle arrays are prepared on the substrate. As UTAMs are fixed during the removal of backside Al and alumina barrier layer, and no polymeric layers are used to support the UTAMs, highly ordered nanoparticle arrays with uniform diameters are obtained over a large area. Figure 4b shows the large-scale highly ordered Au

nanoparticle array with a uniform diameter of about 50 nm. By controlling the pore-widening duration, the diameter of the nanopores can be adjusted, which results in nanoparticle arrays with different size (Figure S4 in Supporting Information). In addition, the diameter of the nanoparticles also can be tuned by controlling the thickness of the UTAM (*i.e.*, the anodization time).²⁶ Because there is no particular requirement for UTAMs in our novel transferring process, UTAMs with different thicknesses and nanopore diameters can be transferred by using this method. The diameter of nanoparticles can be adjusted in the range from sub-10 nm to submicron over large area.^{26,30–32} Also, there is no special requirement in the deposition step, which means many methods can be used to fabricate the nanoparticle arrays such as vapor sublimation, vapor evaporation, electron-beam deposition and sputtering. Furthermore, any material that can pass the nanopores of UTAMs can be fabricated into nanoparticle arrays with tunable dimension by using our method, which shall extensively extend the application of nanoparticle arrays.

Besides nanoparticle arrays, the fabrication of nanomesh with highly ordered nanopore arrays can be realized over large area, just by reversing the procedures of Au deposition and UTAM transferring. Nanomeshes also attracted much attention due to their various applications, such as plasmonics, photovoltaics,

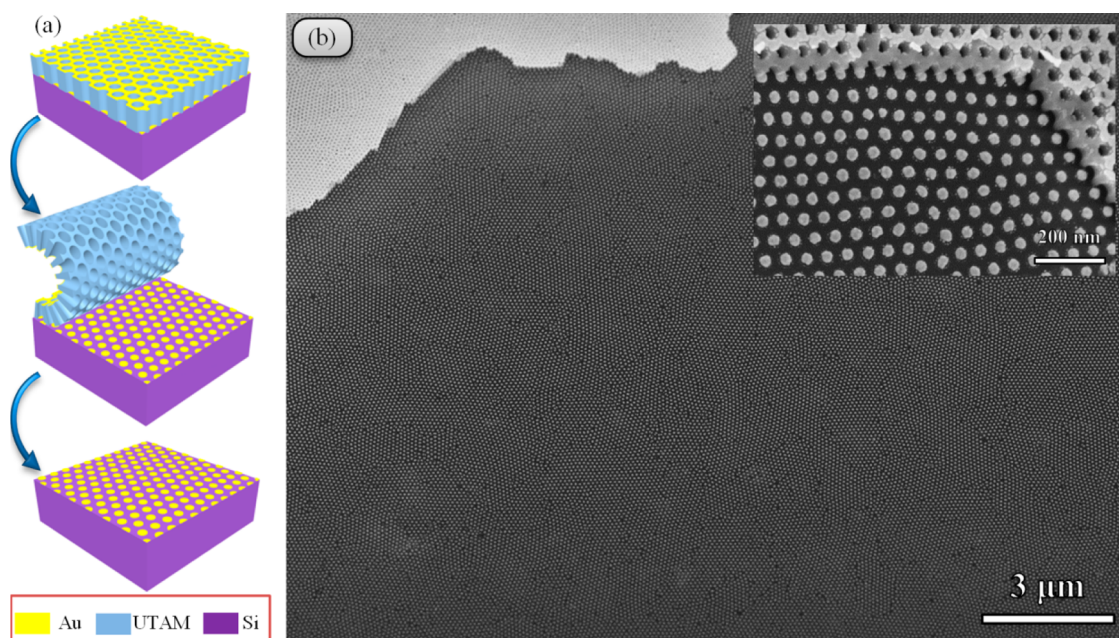


Figure 4. (a) Schematic diagram of the fabrication process of Au nanoparticle arrays on Si wafer by using the UTAM as a shadow mask. (b) Regional and high-resolution (inset) SEM images of Au nanoparticle arrays fabricated on Si wafer with large area, in which parts of the UTAM are remained intentionally.

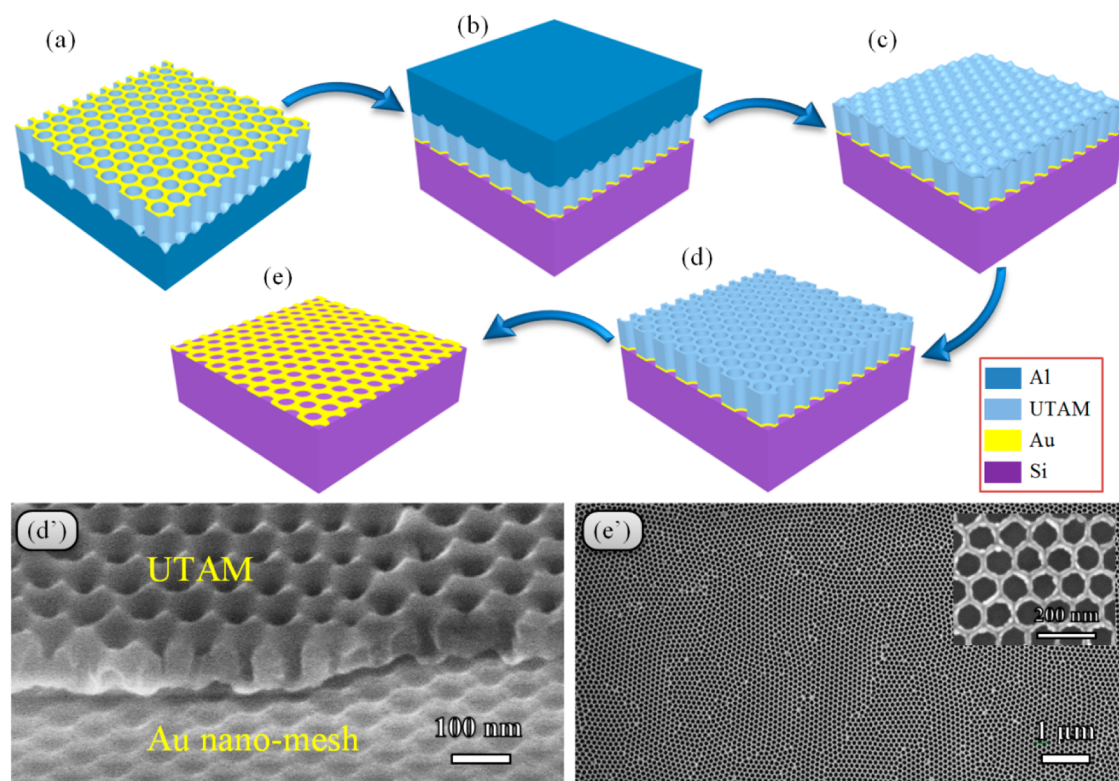


Figure 5. Schematic diagram (a–e) and SEM images (d', e') for the fabrication of Au nanomesh on Si wafer: (a) deposition of Au on UTAM, (b) transferring the Au nanomesh onto Si wafer, (c) removing the residual Al at the backside, (d and d') removal of the barrier layer, and (e and e') Au nanomesh on Si wafer after removing UTAM (the inset of e') is the enlarged view.

metal-assisted chemical etching (MaCE) of Si and shadow mask for etching or transmission of light at sub-wavelength scale.^{33,34} Figure 5a–e shows the schematic diagram for fabrication of Au nanomesh with thickness of about 20 nm on Si wafer. Figure 5d' and 5e' are the

typical SEM images of Au nanomeshes on Si wafer before and after removing UTAM, respectively. By using this method, many materials can be fabricated into nanomeshes over large area. As a proof to demonstrate the applications of metal nanomeshes fabricated by this

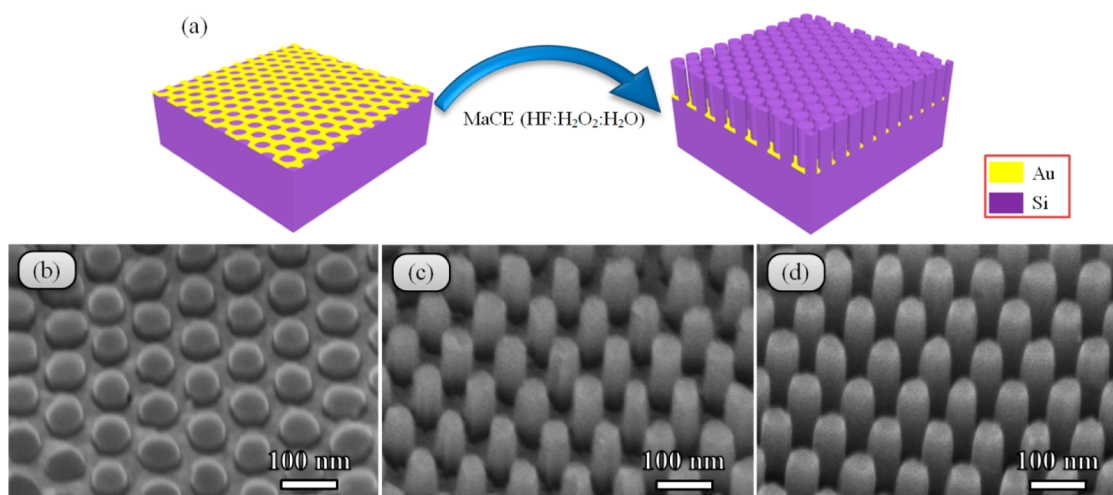


Figure 6. (a) Schematic diagram for the fabrication of Si nanowire array by using Au nanomesh as catalyst mask for Si wafer. SEM images of Si nanowires by etching for (b) 3, (c) 5 and (d) 10 min.

UTAM technique, Si nanowire arrays are fabricated by MaCE method using the obtained Au nanomesh as catalyst to etch Si wafer. Figure 6a outlines this process, in which the whole Si wafer with Au nanomesh (4 in.) is dipped in the etchant ($\text{HF}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$). After the MaCE process, highly ordered Si nanowire arrays are obtained on the surface of Si wafer. During the etching process, the HF in the etching solution dissolves the oxidized Si that formed by oxidation of Si beneath the metal (Au) catalyst with the presence of H_2O_2 . The length of Si nanowires can easily be controlled by monitoring the etching time, as shown in Figure 6b–d.

CONCLUSIONS

In summary, we demonstrate a facile and cost-effective method for the effective transferring of wafer-scale UTAMs onto substrates. Our method guarantees the uniformity and regularity of the nanopore

arrays and prevents the UTAM from external contaminations, due to not using a polymeric supporting layer, the good contact between the UTAM and the substrate, and the fixed UTAM during the entire process. By controlling the thickness of the UTAM, wafer-scale UTAM can be transferred on the desired substrates without any twisting, folding, or cracking, and various nanostructure patterning are achieved over large area by using these transferred UTAMs as templates. Because there is no requirement for the UTAMs, substrates and materials for deposition, various nanostructures including nanoparticle, nanopore (nanomesh) and nanowire arrays can be fabricated on different substrates with tunable and uniform dimension. This work shall pave a way to achieve large-scale nanostructure patterning and provide a platform for various applications of highly ordered nanostructure arrays.

EXPERIMENTAL SECTION

UTAM Preparation. Self-ordered nanoporous UTAM was prepared by two-step anodization of high purity Al foil (99.999%) under a potential of 40 V in 0.3 M oxalic acid at 7 °C. Before anodization, the foil was degreased in acetone, ethanol and rinsed by deionized (DI) water, and then electrochemically polished under a potential of 30 V at 0 °C in a mixed solution contain ($\text{HClO}_4:\text{C}_2\text{H}_5\text{OH}$, v/v = 1:7) with a constant stirring for 2–3 min. Two-step anodization was carried out in our lab-made cell which can hold a 4-in. Al foil. After removing the irregular nanopores obtained by 7 h first anodization (using 6 wt % H_3PO_4 + 1.8 wt % H_2CrO_4 at 60 °C for 8 h), highly ordered nanohollow arrays are left on the top surface of the Al foil. These hollows were adopted as a template for the second anodization, which was carried under the same conditions but using different anodization time (1–8 min) to prepare different thicknesses of UTAMs. The pore diameter of UTAM was tuned by using 5 wt % H_3PO_4 at 30 °C in different time (5–45 min). Then the surface of UTAM was smoothed by using Ar ion milling for 5 min to remove the sharp edges of the nanopores, which can improve the adhesion between the UTAM and the substrate.

UTAM Transferring. The prepared UTAM was transferred onto a standard 4-in. p-Si (100) wafer. In order to improve the adhesion between the UTAM and Si substrate, the wafer was cleaned by Piranha solution ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$, v/v = 3/1) and HF (2%) for 30 and 5 min, respectively, and then thoroughly rinsed by DI water. The UTAM was transferred onto Si wafer by using the same cell unit that was used for anodization, keeping UTAM side connected with the substrate. To get better adhesion, several drops of DI water were dropped between the UTAM and the substrate before placing the UTAM. Finally, the backside Al and the barrier layer of UTAM were completely removed by using aqueous CuCl_2 and 5 wt % H_3PO_4 , respectively.

Au Nanomesh Fabrication. About 20 nm Au was deposited (deposition rate of 0.2 Å/s) onto the top surface of the UTAM (wafer scale) by electron-beam deposition before removal of the backside Al and the barrier layer. The sharp edges on the surface of the prepared UTAM also were smoothed by using argon ion milling to get a smooth and a uniform UTAM. Then the Au nanomesh was transferred onto the substrate according to the similar step of the transferring of UTAM, followed by 2 s etching in a mixed solution of ($\text{HF}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, v/v/v = 50/25/175) to remove the UTAM completely.

Au Nanoparticle Arrays Fabrication. After transferring the UTAM onto Si wafer, Au nanoparticle arrays were prepared by deposition of about 20 nm Au (deposition rate of 0.2 Å/s) on this transferred UTAM which acts as a shadow mask for Si wafer. Finally, the UTAM was removed by using a commercial tape.

Silicon Nanowire Arrays Fabrication. After placing the Au nanomesh onto Si wafer, Si nanowire arrays were fabricated by immersing Si wafer with Au nanomesh in the etching solution (HF:H₂O₂:H₂O, v/v/v = 50/25/175). The growth of the nanowires was controlled by the etching times.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Photographs of the cell unit, transferring processes and free-standing 4-in. wafer scale UTAM, and SEM micrographs of UTAMs with different pore diameters (45, 60, 75 and 90 nm) and Au nanoparticle arrays with different sizes (45, 60, 75 and 90 nm). The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b03789.

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